EVOLVABLE, RECONFIGURABLE HARDWARE FOR FUTURE SPACE SYSTEMS

A. Stoica, R.S. Zebulum, D. Keymeulen, M. I. Ferguson, A. Thakoor
Jet Propulsion Laboratory, California Institute of Technology
and
Xin Guo, Chromatech

adrian.stoica@jpl.nasa.gov

Abstract – This paper overviews Evolvable Hardware (EHW) technology, examining its potential for enhancing survivability and flexibility of future space systems. EHW refers to self-configuration of electronic hardware by evolutionary/genetic search mechanisms. Evolvable Hardware can maintain existing functionality in the presence of faults and degradations due to aging, temperature and radiation. It can also configure itself for new functionality when required for mission changes or encountered opportunities. The paper illustrates hardware evolution in silicon using a JPL-designed programmable device reconfigurable at transistor level as the platform and a genetic algorithm running on a DSP as the reconfiguration mechanism. Rapid reconfiguration allows convergence to circuit solutions in the order of seconds. The experiments demonstrate functional recovery from faults as well as from degradation at extreme temperatures indicating the possibility of expanding the operational range of extreme electronics through evolved circuit solutions.

1. INTRODUCTION

The idea behind evolutionary circuit synthesis/design and Evolvable Hardware (EHW) is to employ a genetic search/optimization algorithm that operates in the space of all possible circuits and determines solution circuits that satisfy imposed specifications, including target functional response, size, speed, power, etc. In the narrow sense, EHW refers to self-reconfiguration of electronic hardware by evolutionary/genetic reconfiguration mechanisms. In a broader sense, EHW refers to various forms of hardware from sensors and antennas to complete evolvable space systems that could adapt to changing environments and, moreover, increase their performance during their operational lifetime.

EHW can bring some key benefits to spacecraft survivability, adaptation to new mission requirements and mission reliability. Firstly, EHW can help preserving existing functions, in conditions where hardware is subject to faults, aging, temperature drifts and radiation. The environmental conditions, in particular the extreme temperatures and radiation effects, can have catastrophic impacts on the spacecraft. Interstellar missions or extended missions to other planets in our solar system, with lifetimes in excess of 100 years, are great challenges on the on-board electronics. Secondly, new functions can be generated when needed (more precisely, new hardware configurations can be synthesized to provide required functionality). Finally, EHW and reconfigurable electronics provide additional protection against design mistakes that may be found after launch. Design errors can be circumvented during the mission either by human or evolutionary driven circuit reconfiguration. Figure 1 illustrates these ideas.

One example of area where EHW can bring benefit is in-situ planetary exploration. In-situ planetary exploration requires extreme-temperature electronics able to operate in low temperatures, such as below –220^{o}C on Neptune (-235^{o}C for Triton and Pluto) or high temperatures, such as above 470^{o}C as needed for operation on the surface of Venus. Extrapolations of current developments indicate that hot electronics technology for >400^{o}C environments may not be ready in time for the 2006-2007 missions, except possibly for "grab-and-go" or "limited life" operations. For extended missions, innovative

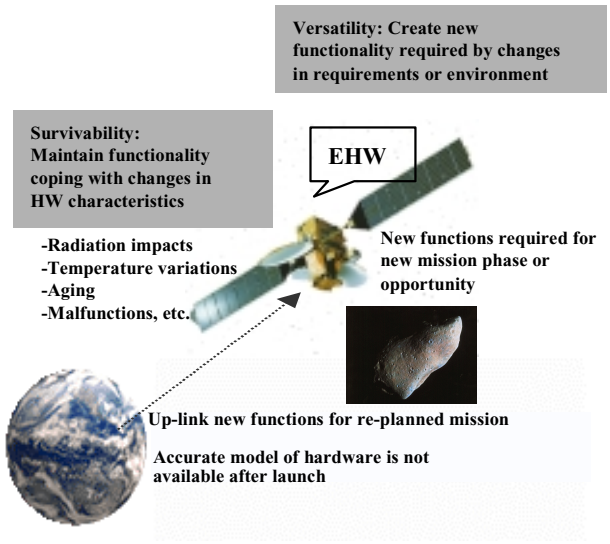


Figure 1: EHW can contribute to increase spacecraft survivability and flexibility.

approaches are needed. Terrestrial applications include combustion systems, well logging, nuclear reactors and dense electronic packages. In this paper we propose the use of reconfigurable chips, which allow for a large number of topologies to be programmed in-situ, allowing adaptation to extreme temperatures

The experiments in this paper illustrate hardware recovery from faults and expansion of the operational range of hot electronics in the vicinity of 320°C. In the case of faults, evolution finds circuit solutions that bypass faulty areas. In the case of extreme temperatures, evolution finds circuit solutions interconnecting the components in new ways that better exploit their characteristic curves at that temperature. In addition, we present experiments that show the evolution of adaptive (tunable) filters and review an application on the evolution of reconfigurable antennas.

The paper is organized as follows. Section 2 reviews EHW main aspects, including reconfigurable devices for EHW, reconfiguration mechanisms for hardware evolution and EHW testbeds. Section 3 describes experiments on the evolutionary design of analog circuits. Section 4 describes experiments on electronic survivability through evolution, including evolutionary recovery at extreme temperatures and electronic circuits self-repair. Section 5 describe one experiment on evolvable sensing. Section 6 concludes the work.

2. EVOLVABLE HARDWARE

Currently, the evolutionary search for a circuit solution is performed either using software simulations[1,2,3] or directly in hardware on reconfigurable chips[4]. However, software simulations take too long for practical purposes, since the simulation time for one circuit is multiplied by the large number of evaluations required by evolutionary algorithms. In addition the resulting circuit may not be easily implemented in hardware, unless implementation constraints are imposed during evolution. Hardware evaluations can reduce by orders of magnitude the time to get the response of a candidate circuit, potentially reducing the evolution time from days to seconds [4].

Hardware evaluations commonly use commercial re-configurable devices, such as Field Programmable Gate Arrays (FPGA) or Field Programmable Analog Arrays (FPAA) [5,6]. These devices, designed for several applications other than EHW, lack evolution-oriented features, and, in particular the analog ones, are sub-optimal for EHW applications.

2.1 Evolutionary Oriented Reconfigurable Architectures

To best support EHW several aspects for evolution-oriented reconfigurable architectures

(EORA) must be considered. The granularity of the programmable chip is an important feature. A first limitation of commercial FPGAs and FPAAs is their coarse granularity. From the EHW perspective, it is interesting to have *programmable granularity*, allowing the sampling of novel architectures together with the possibility of implementing standard ones. The optimal choice of elementary block type and granularity is task dependent. At least for experimental work in EHW, it appears a good choice to build reconfigurable hardware based on elements of the lowest level of granularity. Virtual higher-level building blocks can be considered by imposing programming constraints. EORA should also be *transparent architectures*, allowing the analysis and simulation of the evolved circuits. They should also be robust enough not to be damaged by any bit-string configuration existent in the search space, potentially sampled by evolution. Finally EORA should allow evolution of both analog and digital functions.

This paper describes the Field Programmable Transistor Array (FPTAs) chips designed at JPL, and particularly targeted for EHW experiments. The first versions of the FPTA (FPTA-0 and FPTA-1) relied on a cell with 8 transistors interconnected by 24 switches[5]. They were used to demonstrate intrinsic evolution of a variety of circuits, including logical gates, transconductance amplifiers, computational circuits, etc [1,2,3,7].

The most recent version, FPTA2, is a second generation reconfigurable mixed signal array chip whose cells can be programmed at the transistor level. The chip architecture consists of an 8x8 matrix of re-configurable cells. The chip can receive 96 analog/digital inputs and provide 64 analog/digital outputs. Each cell is programmed through a 16 bits data bus/9 bits address bus control logic, which provides an addressing mechanism to download the bit-string of each cell. A total of 5000 bits is used to program the whole chip. An array of 16x8 photo-detectors, distributed within the cells, is also integrated on chip. It is the first chip integrating reconfigurable processing circuitry with sensing. The FPTA-2 cell consists of 14 transistors connected through 44 switches and it is able to map different building blocks for analog processing, such as two and three stages OpAmps, logarithmic photo-detectors, or Gaussian computational circuits. Figure 2 shows the details of the FPTA cell for the first and for the latest version of the FPTA chip.

2.2. Evolutionary Reconfiguration Mechanisms

The genetic search in EHW is tightly coupled with a coded representation that associates each circuit to a "genetic code" or chromosome. The simplest representation of a chromosome is a binary string, a succession of 0s and 1s that encode a circuit. The status of the switches (ON or OFF) determines a circuit topology and consequently a specific response. Thus, the topology can be considered as a function of switch states, and can be represented by a binary sequence, such as “1011…”, where a ‘1’ is associated to a switch turned ON and a ‘0’ to a switch turned OFF. The main steps of evolutionary synthesis are illustrated in Figure 3.

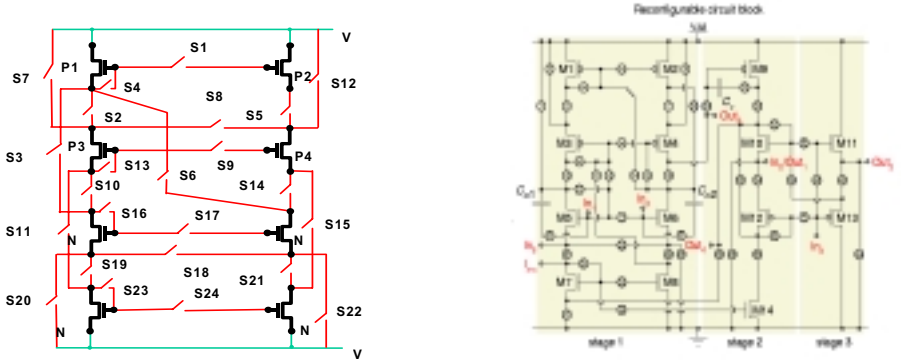


Figure 2. FPTA cell topology as used in two FPTA chips (FPTA-0 in the left , FPTA-2 chip in the right).

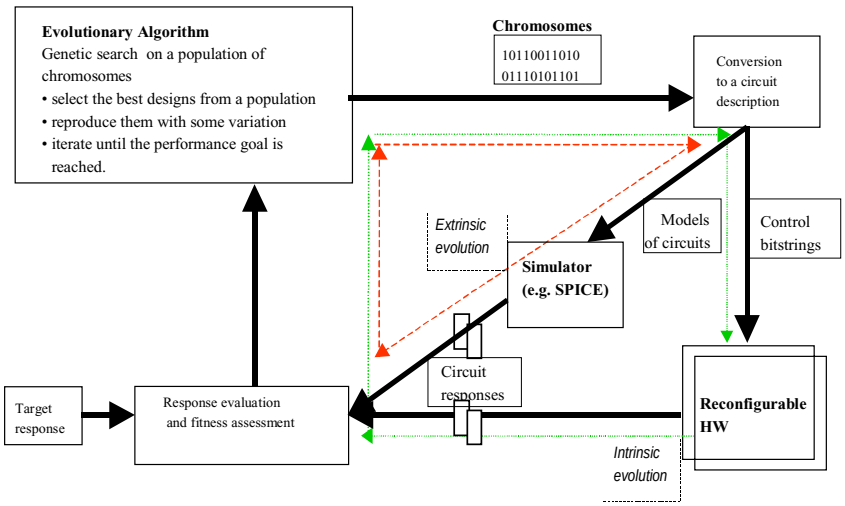


Figure 3: Main steps for the evolutionary synthesis of electronic circuits.

First, a population of chromosomes is randomly generated. The chromosomes are converted into circuit models for evaluation in SW (extrinsic evolution) or into control bitstrings downloaded to programmable hardware (intrinsic evolution). Circuit responses are compared against specifications, and individuals are ranked based on how close they come to satisfying them. In preparation for a new iteration, a new population of individuals is generated from the pool of best individuals in the previous generation. This is subject to a probabilistic selection of individuals from a best individuals pool, followed by two operations: random swapping of parts of their chromosomes, the *crossover* operation, and random flipping of chromosome bits, the *mutation* operation. The process is repeated for several generations, resulting in increasingly better individuals. Randomness helps to avoid getting trapped in local optima. Monotonic convergence (in a loose Pareto sense) can be forced by unaltered transference to the next generation of the best individual from the previous generation. There is no theoretical guarantee that the global optimum will be reached in a useful amount of time; however, the evolutionary/genetic search is considered by many to be the best choice for very large, highly unknown search spaces. The search process is usually stopped after a number of generations, or when closeness to the target response has reached a sufficient degree. One or several solutions may be found among the individuals of the last generation.

2.3 Evolvable Hardware Testbeds

The JPL Evolvable Hardware Testbed was developed to support both SW and HW evaluations (extrinsic/intrinsic). The SW resources rely on a 128-processor parallel machine of SGI Origin running multiple copies of SPICE. The HW resources are built around National Instruments LabView, associated data acquisition boards, signal generators, and other equipment [8].

A stand alone board level Evolvable System (SABLES) was developed for autonomous portable experiments is a stand-alone platform, integrating the FPTA-2 and a DSP implementing the Evolutionary Platform (EP) as shown in Figure 4. The system is stand-alone and is connected to the PC only for the purpose of receiving specifications and communicating back the results of evolution for analysis.

Figure 4: Block diagram of a simple stand-alone evolvable system.

The evolutionary algorithm was implemented in a DSP that directly controlled the FPTA-2, together forming a board-level evolvable system with fast internal communication ensured by a 32-bit bus

operating at 7.5MHz. Details of the EP were presented in [9]. Over four orders of magnitude speed-up of evolution was obtained on the FPTA chip compared to SPICE simulations on a Pentium processor (this performance figure was obtained for a circuit with approximately 100 transistors; the speed-up advantage increases with the size of the circuit).

3. EVOLUTIONARY EXPERIMENTS: AUTOMATIC SYNTHESIS OF ANALOG CIRCUITS

The first demonstration of SABLES is reported in [4,9]. A half-wave rectifier circuit was evolved in about 20 seconds after processing a population of 100 individuals running for 200 generations. The testing of candidate circuits is made for an excitation input of 2kHz sine wave of amplitude 2V. A computed rectified waveform of this signal is considered as the target. The fitness function rewards those individuals exhibiting behavior closer to target (using a simple sum of differences between the response of a circuit and target) and penalizes those farther from it. In this experiment only two cells of the FPTA were allocated.

Figure 5 displays snapshots of evolution in progress, illustrating the response of the best individual in the population over a set of generations. The first caption shows the best individual of the initial population, while the subsequent ones show the best after 5, 50 and 82 generations. The solution is shown on the right.

In another experiment we evolve an autonomous tunable filter[10]. In this experiment, the linear combination of two source signals (10kHz and 20kHz) was applied to the FPTA-2 chip. The source signals are unknown to the evolutionary system, in the sense that no information about the input signal is used by the fitness evaluation function. The fitness criteria employed here is to amplify the strongest tone at the output and attenuate the weakest one, which we *respectively* assume to be signal and noise. Four cells of the chip were used in the experiment. Figure 6 summarizes the performance of the evolved circuit. Initially, the 10kHz tone has about twice the amplitude of the 20kHz tone. The circuit output increases the *"signal/noise*" ratio from 4.1dB to 16.9dB. In this case, the 10kHz tone is attenuated by 2.86dB, while the 20kHz tone is attenuated by 15.8dB. If we invert the source signal ratios, it is observed that evolution *autonomously* change the circuit configuration: the *"signal/noise*" ratio increases from 10.8dB to 18.5dB. In this case, the 10kHz tone is attenuated by 12.5dB, while the 20kHz tone is attenuated by 4.8dB. It can be observed that the performance is better in the first case.

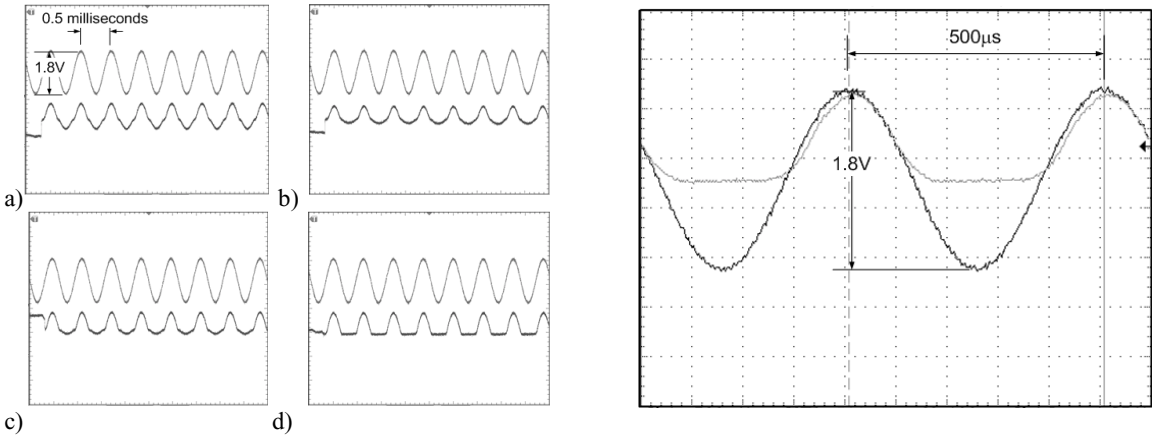


Figure 5. Evolution of a halfwave rectifier showing the response of the best individual of generation a) 1, b) 5, c) 50 and finally the solution at generation d) 82. The final solution, which had a fitness value less than 4500, is illustrated on the right.

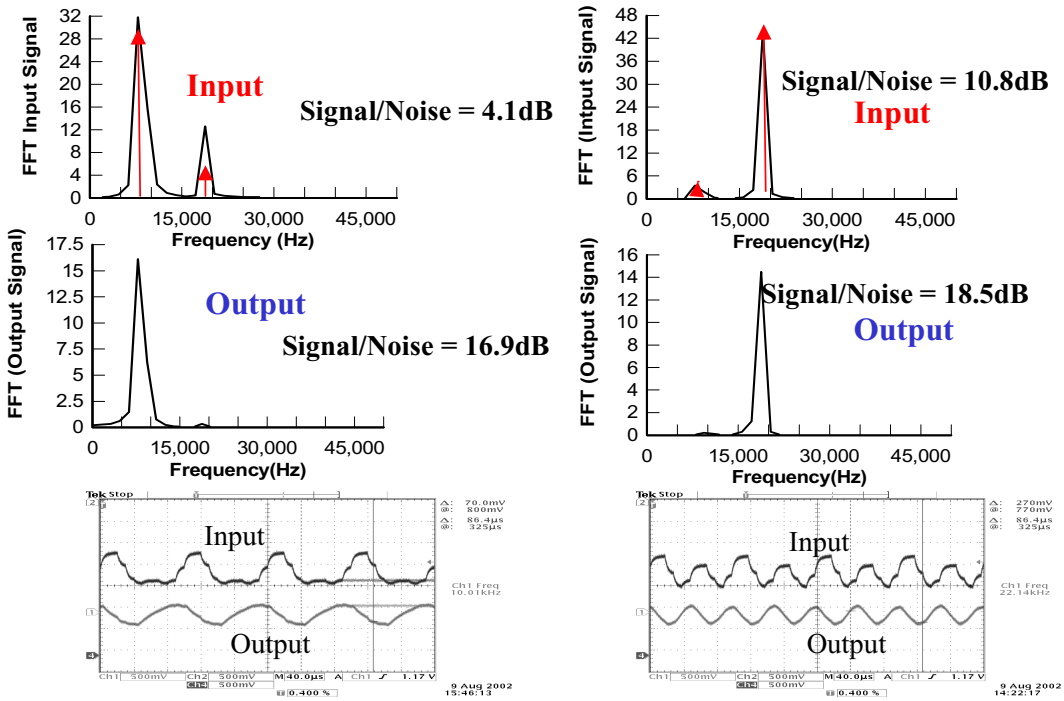


Figure 6. The left side displays data for the first experiment (10kHz tone has twice the amplitude of the 20kHz tone): FFT of the input (top), FFT of the output (middle) and time domain behavior of input and output. The right side illustrates the same information for the case in which the 20kHz tone has higher amplitude.

Filters that can autonomously change their frequency response may have a major impact on missions exploring unknown environments, which must adapt to changing and uncertain conditions.

4. EVOLUTIONARY ENABLED ELECTRONIC SURVIVABILITY

4.1 Extreme Temperatures

For the purpose of the temperature experiments we have constructed special boards, which were inserted in liquid nitrogen for low temperatures or exposed to a hot air jet for high temperatures. Both experiments were carried out using the FPTA-0 chip. In the case of low temperatures, the DC transfer function of a Gaussian circuit mapped onto the FPTA-0 chip was recovered by evolutionary synthesis, after being deteriorated by the low (-196^{o}C) temperature [2].

In the case of high temperatures, experiments were carried out immersing the FPTA chip in temperature controlled environments at high temperature (up to +330^{o}C). Figure 7 shows a picture of the high-temperature testbed. A focused hot air jet hits the chip die, being able to increase its temperature up to 1000^{o}C. Due to silicon limits, experiments were performed with temperatures up to 330^{o}C. The excitation signals come from signal generators and the circuit output is read back by LabView. The sequence of steps was: (1) Implement a human design or evolve a new design for desired function at 27^{o}C. (2) Expose chip to high temperature and observe degraded response (3) Apply evolution to obtain a new circuit solution that recovers functionality. In these experiments the following evolutionary parameters were used: Population size of 50, running for 200 generations; mutation rate of 8% and crossover rate of 30%. The case studies tacked was the evolution of a NOR gate, as shown in Figure 8.

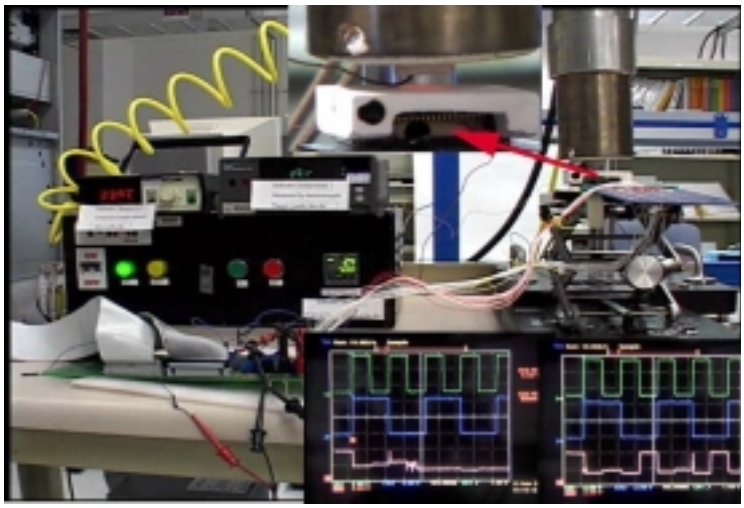
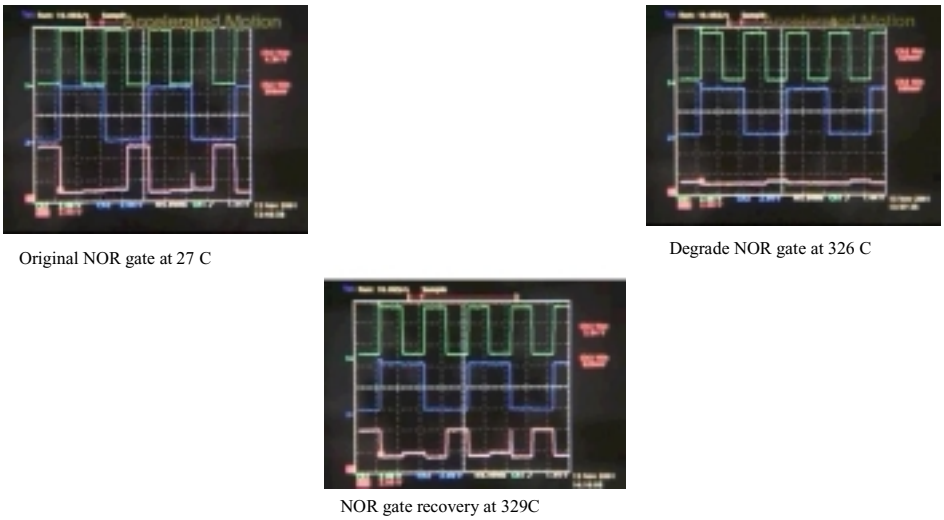


Figure 7: High temperature experimental testbed.

Figure 8 presents an oscilloscope capture that illustrates the degradation with temperature in response of a NOR gate, and the recovery by evolution. One should remark that the evolved solutions, while adapted to the extreme temperature, were not necessarily preserving functionality when the temperature was being brought back to room temperature.

4.2. Self-Repair of Electronic Circuits

The evolution and self-repair of an analog multiplier is shown in this section[1]. This circuit was evolved using two cascaded FPTA cells connected by 6 switches, comprising 88 bits. The circuit schematic is shown in Figure 9. After generation 59, when the best individual is sufficiently close to the target, one fault is induced by cutting one connection between the two FPTA cells, degrading the multiplier response. After 20 generations the GA is able to recover the desired circuit functionality. Figure 9 compares the circuit output with the target response during the overall experiment, as well as the fitness function. The experiment used the FPTA-0 and the National Instrument testbed.



Original NOR gate at 27 C

Degrade NOR gate at 326 C

NOR gate recovery at 329C

Figure 8: Original NOR gate at 27°C (upper left) and degraded behavior at 326°C (upper right). At the bottom, NOR gate recovered by evolution at 329°C.

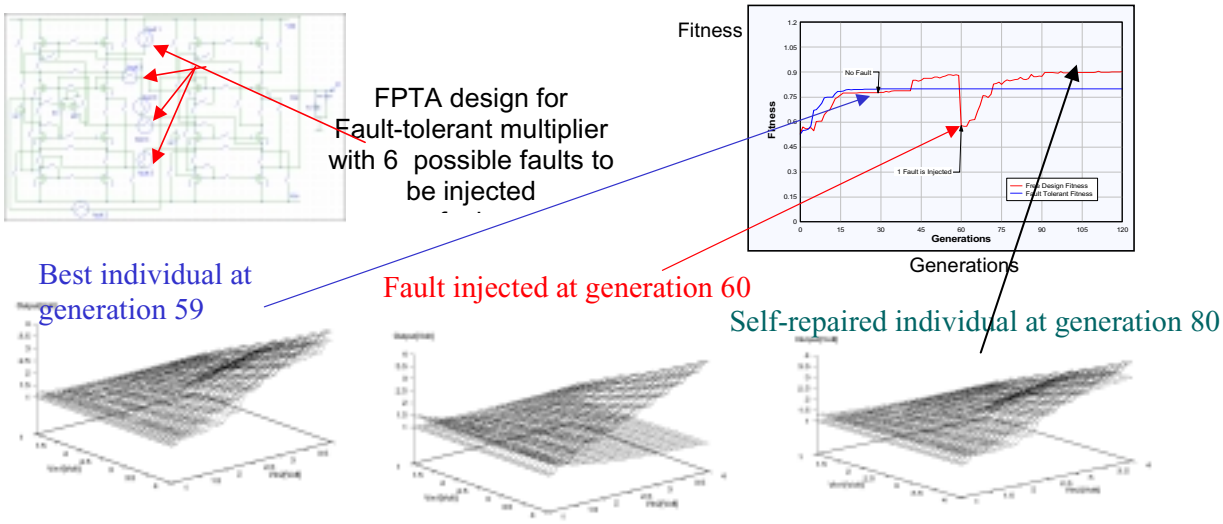


Figure 9: Schematic of the cascaded cell configuration used in the experiment (upper left). Fitness functionis shown at the upper right. Circuit response compared to target before the fault (generation 59) after the fault (generation 60) and after recovery (generation 80).

5. EVOLVABLE SENSING

The main idea in evolvable sensing is to replace analog dedicated circuits between sensors and analog to digital converters with flexible and adaptable circuits that could be reconfigured to optimize signal processing in a variety of contexts. Also included in reconfigurable sensing is the use of reconfigurable sensor elements such as the reconfigurable antennas. In the following we describe an experiment with a reconfigurable antenna.

The objective of the experiment is to show that an evolved reconfigurable antenna, in-situ adapted to environment, can outperform conventional antennas. The re-configurable antenna topology consisted of a printed circuit board with traces connected by 48 relay switches and one feed point. The dimensions of the antenna provided a wavelength of 2.4GHz. A Genetic Algorithm (GA) was used to optimize the antenna configuration by programming the switch states. In order to evaluate the antenna performance, the evolutionary algorithm used a Received Signal Strength Indicator (RSSI) to measure the antenna performance (Figure 10). In one particular

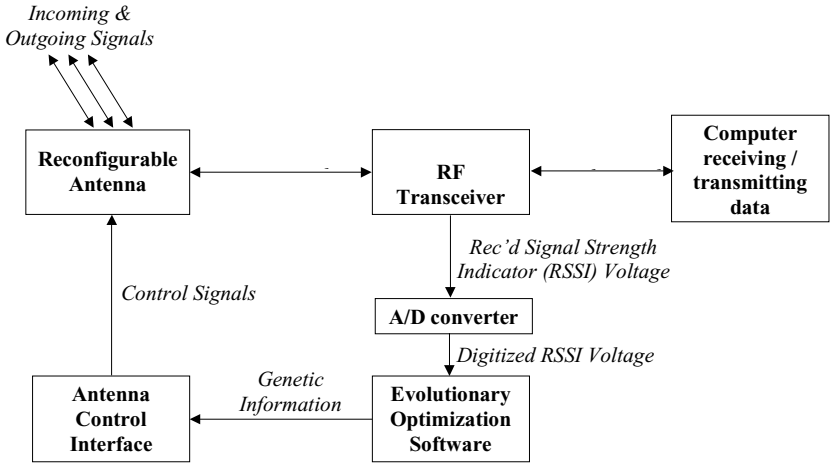


Figure 10: Block Diagram Evolvable Antenna System. (JPL funded work by Derek Linden (dlinden@lindenir.com).

experiment, a ½ wave dipole antenna transmitted a 2.4GHz signal, and the evolvable antenna was placed about 3m from the receiver. Different experiments were performed changing the orientation of the evolvable antenna and placing barriers between transmitter and receiver antennas. It has been verified from the experiments that, for the different antenna orientations and experimental setup, the evolvable antenna showed better gain comparing to a 5/8-wavelangth fixed antenna used for comparison [11].

6. CONCLUSIONS

The above experiments ilustrate the power of EHW to synthesize new functions and to recover degraded functionality due to faults or extreme temperatures.

EHW has the potential to be the underlying technology behind the avionics infrastructure of the space systems for 2020 and beyond. Future avionics may evolve not only electronics but also smart optical/structural/thermal subsystems through reconfiguration and morphing. EHW technology will enable:

–Reconfiguration for multiple functionality of avionics systems using the existing resources.
–Adaptation for new needed functionality
–Fault-tolerance and self-healing for recovering functionality by rerouting around damaged components and reusing components with modified/altered characteristics in new circuit topologies.
–Autonomous avionics through self-configuration.

Acknowledgements

The research described in this paper was performed at the Center for Integrated Space Microsystems, Jet Propulsion Laboratory, California Institute of Technology and was sponsored by the Defense Advanced Research Projects Agency (DARPA) and the National Aeronautics and Space Administration (NASA).

References

[1] D. Keymeulen, A. Stoica, R. Zebulum, Raoul Tawel, Taher Daud, Anil Thakoor. Fault-Tolerant Evolvable Hardware using Field Programmable Transistor Arrays. In *IEEE Transactions on Reliability*, Special Issue on Fault-Tolerant VLSI Systems, vol. 49, No. 3, 2000 September, pp. 305-316,. IEEE Press.

[2] Stoica, D. Keymeulen, and R. Zebulum, "Evolvable Hardware Solutions for Extreme Temperature Electronics", Third NASA/DoD Workshop on Evolvable Hardware, Long Beach, July, 12-14, 2001, (pp.93-97), IEEE Computer Society .

[3] Stoica, R. Zebulum, D. Keymeulen and J. Lohn, "On Polymorphic Circuits and Their Design Using Evolutionary Algorithms" In Proceedings of IASTED International Conference on Applied Informatics (AI2002) 18 –21 February, 2002, Innsbruck, Austria.

[4] Adrian Stoica, Ricardo S. Zebulum, M.I. Ferguson, Didier Keymeulen, Vu Duong, "Evolving Circuits in Seconds: Experiments with a Stand-Alone Board Level Evolvable System". 2002 NASA/DoD Conference on Evolvable Hardware, Alexandria Virginia, USA, July 15-18, 2002, pp. 67-74IEEE Computer Society.

[5] Stoica, Adrian Stoica, Ricardo Zebulum, Didier Keymeulen, Raoul Tawel, Taher Daud, and Anil Thakoor. Reconfigurable VLSI Architectures for Evolvable Hardware: from Experimental Field Programmable Transistor Arrays to Evolution-Oriented Chips. *IEEE Transactions on VLSI*, IEEE Press , Volume 9, Number 1, ISSN 1063-8210, pp. 227-232, February 2001.

[6] Santini, C., Zebulum, R., et. Al, "PAMA – Programmable Analog Multiplexer Array", published in Proc. of the Third NASA/DoD workshop on Evolvable Hardware, Long Beach, CA, July, 2001.

[7] A. Stoica, D. Keymeulen, A. Thakoor, T. Daud, G. Klimech, Y. Jin, R. Tawel, V. Duong. "Evolution of Analog Circuits on field Programmable Transistor Arrays". In J Lohn et al.(eds.),Proceedings of NASA/DoD Workshop on Evolvable Hardware (EH2000), July 13-15,2000, (pp.99-108). Palo Alto, CA, USA. IEEE Computer Society.

[8] D. Keymeulen, Gerhard Klimeck, R. Zebulum, Adrian Stoica, Yili Jin, Carlos-Salazar Lazaro. "EHWPack: an Evolvable Hardware Environment using the Spice Simulator and the Field Programmable Transistor Array". In the Proceedings of ANNIE'2000 (Smart Enginering System Design), St. Louis, MO, pp. 233-338, ASME Press November 5-8, 2000.

[9] M.I. Ferguson, A. Stoica, D. Keymeulen and R. Zebulum and V. Duong, "An Evolvable Hardware Platform based on DSP and FPTA". In Proceedings of the Genetic and Evolutionary Computation Conference (GECCO2002), July 7-11, 2002, USA. Memlo Park, CA: AAAI Press.

[10] Zebulum, R.S. , Stoica, A., Keymeulen, D., M.I Ferguson, Duong, V., Vorperian, V., "Automatic Evolution of Tunable Filters Using SABLES", submitted for the 2003 International Conference on Evolvable Systems (ICES) to be held in Norway, March, 2003.

[11] D.S. Linden, " Optimizing Signal Strength In-Situ Using an Evolvable Antenna System", 2002 NASA/DoD Conference on Evolvable Hardware, Alexandria Virginia, USA, July 15-18, 2002, pp. 147-151, IEEE Computer Society.